

Status of the Test Beam DAQ System

November 2002

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Overwiev of activities

- Strategy for pixel calibration and development of appropriate code
- Redesign of the DAQ interface (rationalization of commands and functionalities taking advantage of acquired expertise)
- Progresses and problems encountered during continued tests of the system
- Progress about data format (nothing new)

Strategy for pixel calibration

The basic idea is to define a new header word to specify that data collected are of kind CALIBRATION

Marker	Number of pulses sent		Current threshold setting
	Row	Column	Pulse height
	Row	Column	Pulse height



	Row	Column	Pulse height
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When the event builder detects this type of marker, discards the time-stamp (BCO) information and builds the event just based on row and column number, thus producing the needed threshold curves.

We are still debating with Gabriele how to best reproduce his past calibration technique with this new approach in the context of our new DAQ, so more details will be given at the next meeting

Development of a new interface

We are in the process of developing a new interface to the test beam pixel DAQ

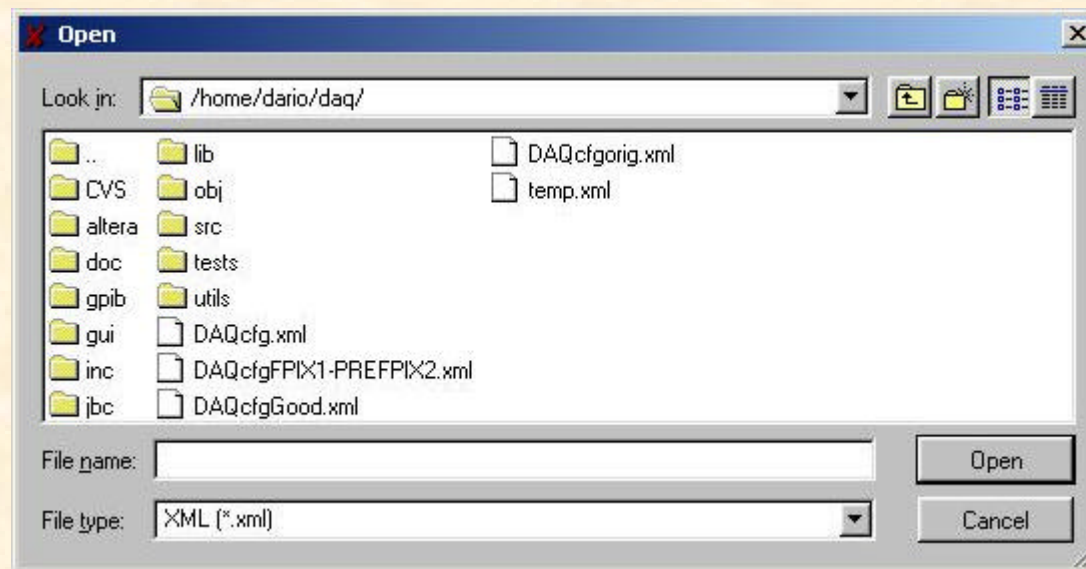
This is because after the first stage of development we have now a system that works as needed for what concerns its internal functionality, but we definitely need to rationalize the public interface (the GUI) so that taking data only needs the push of, at most, a couple of buttons.

There will be one single widget, basically divided in two parts:

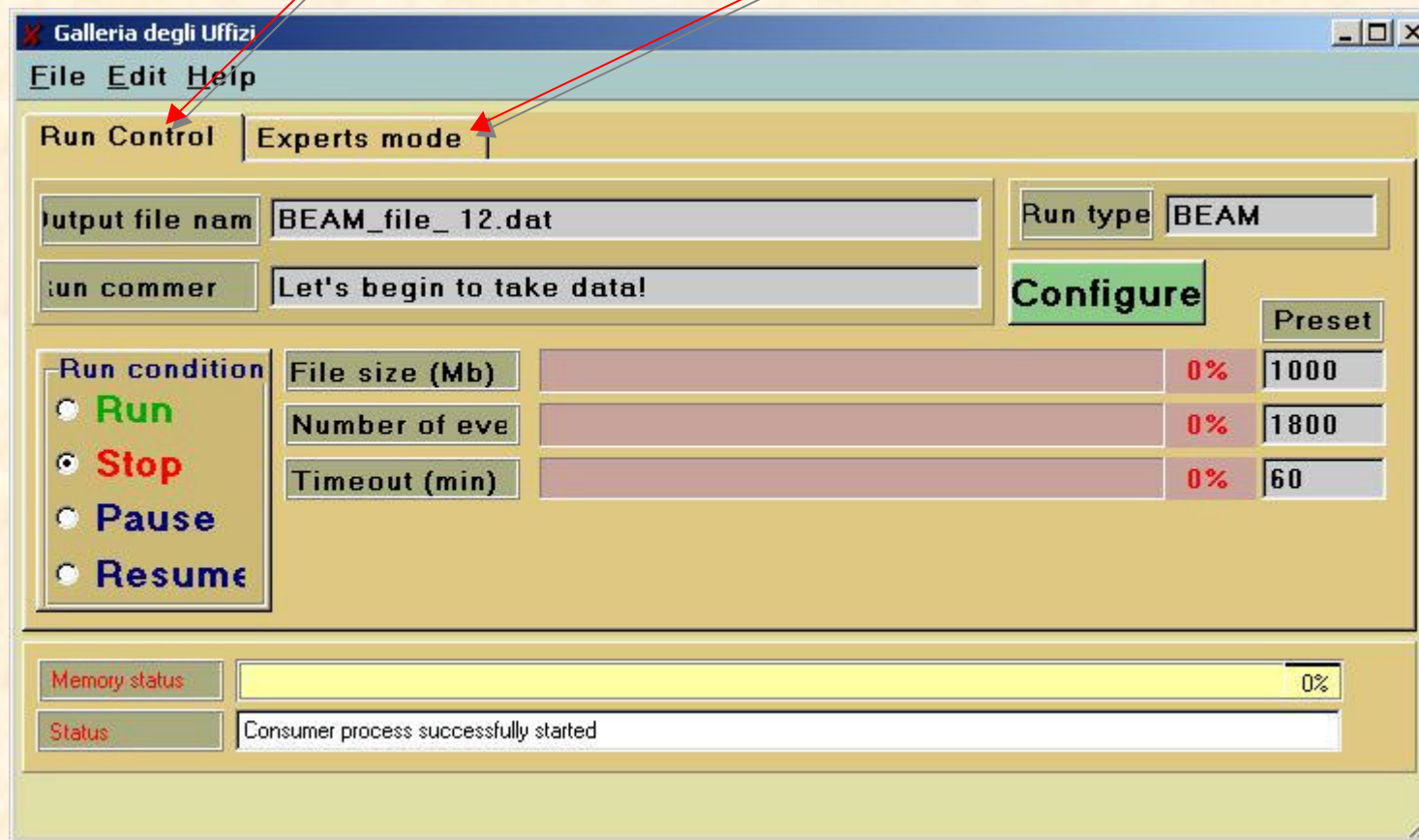
- a normal data taking mode (for the casual user)
- an expert mode with all the needed diagnostic tools (currently under development)

The new GUI

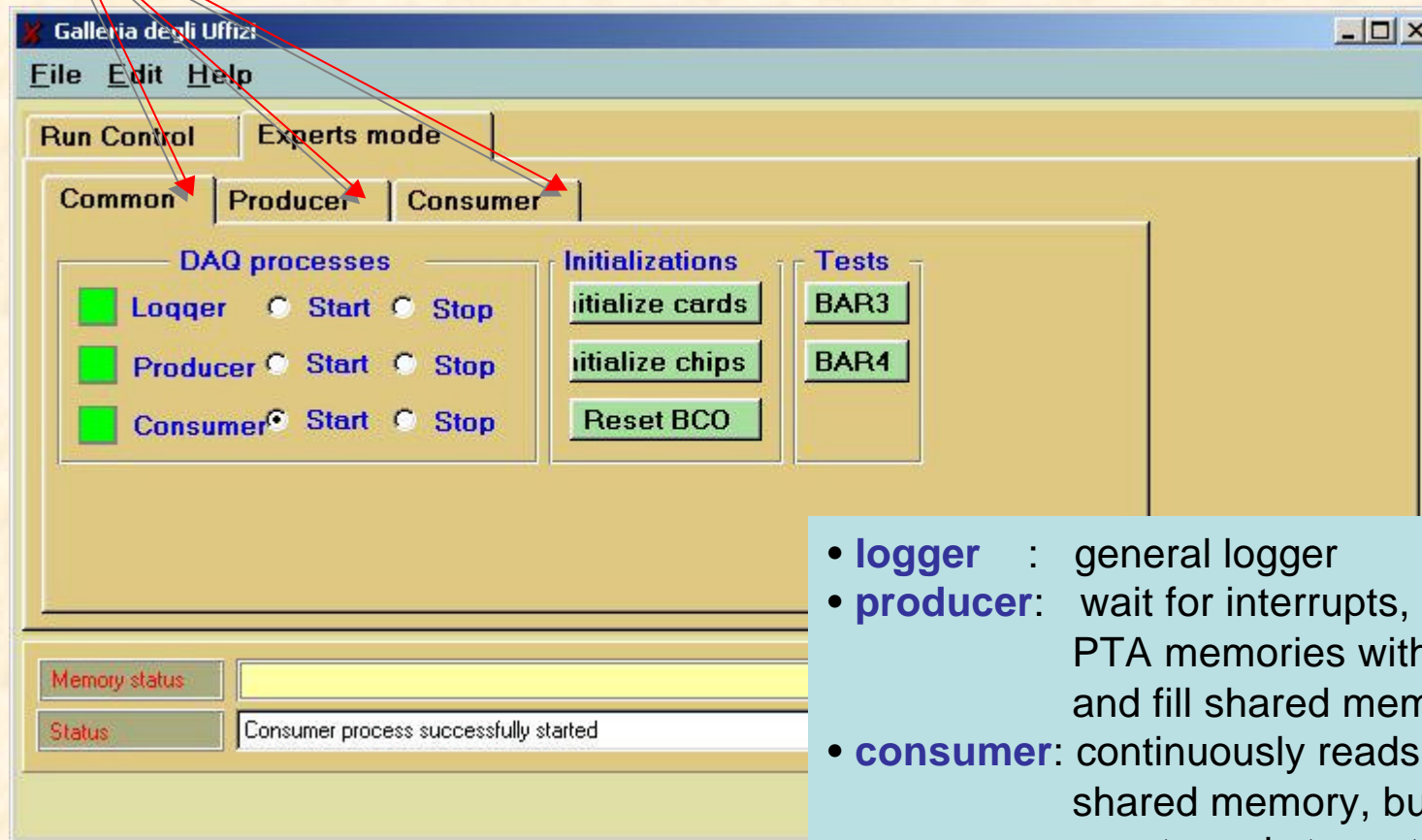
The persistent repository of the whole internal configuration of the DAQ state is the xml configuration file. First thing happens when the DAQ starts is the pop-up of a explorer window to allow users specify which file to use.



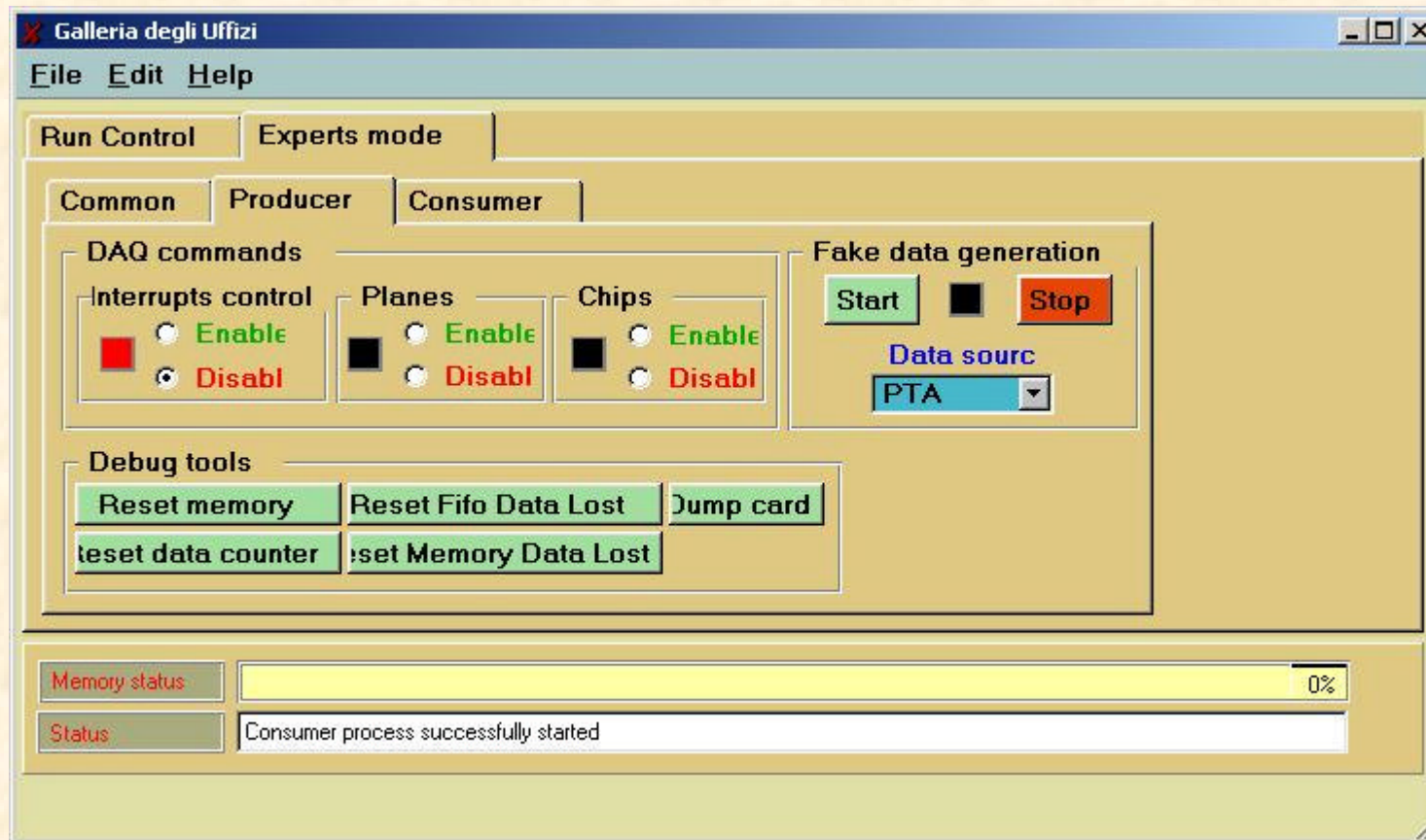
Two tabs: **normal run mode** and **experts only mode**

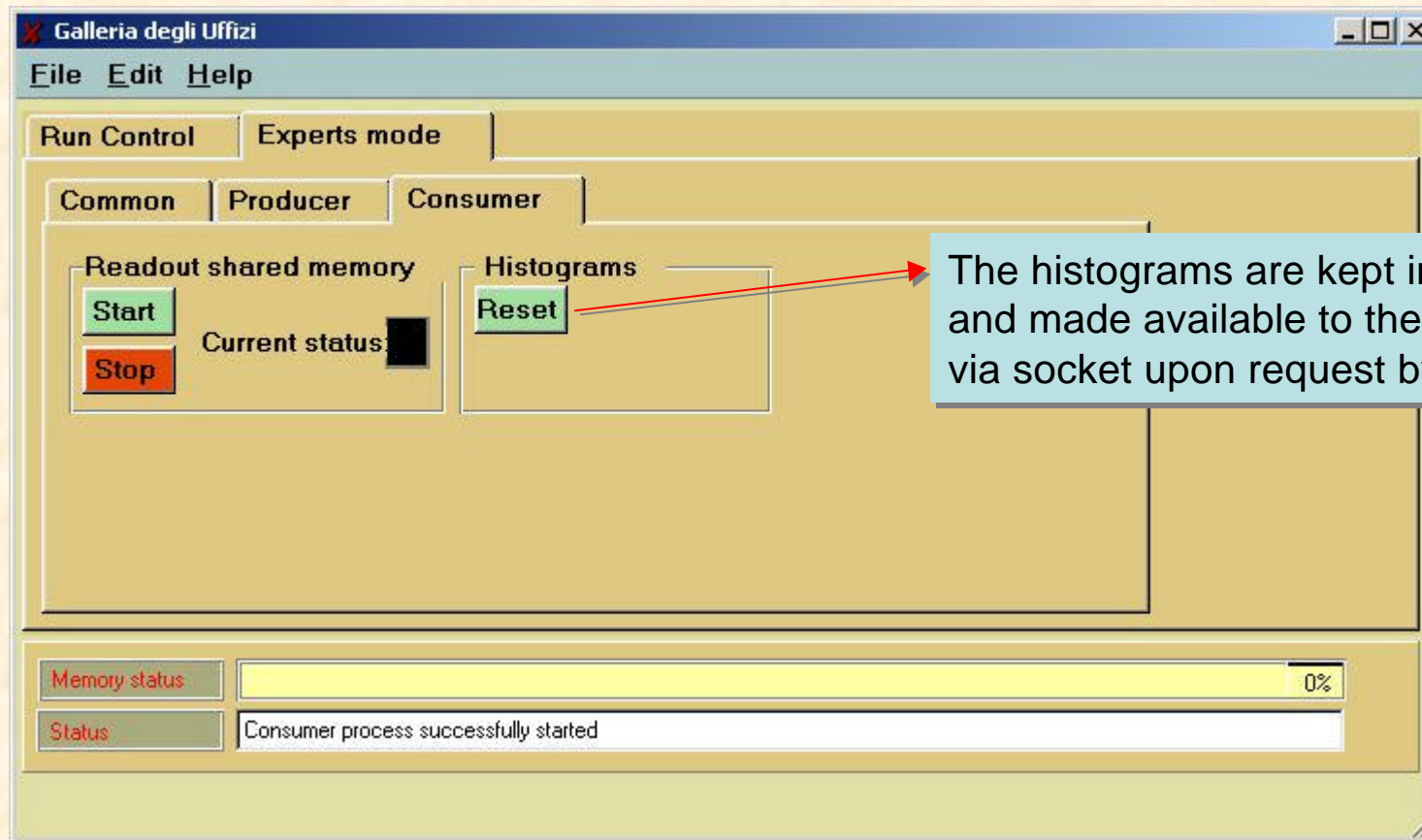


Three tabs, one for each basic process involved in the DAQ

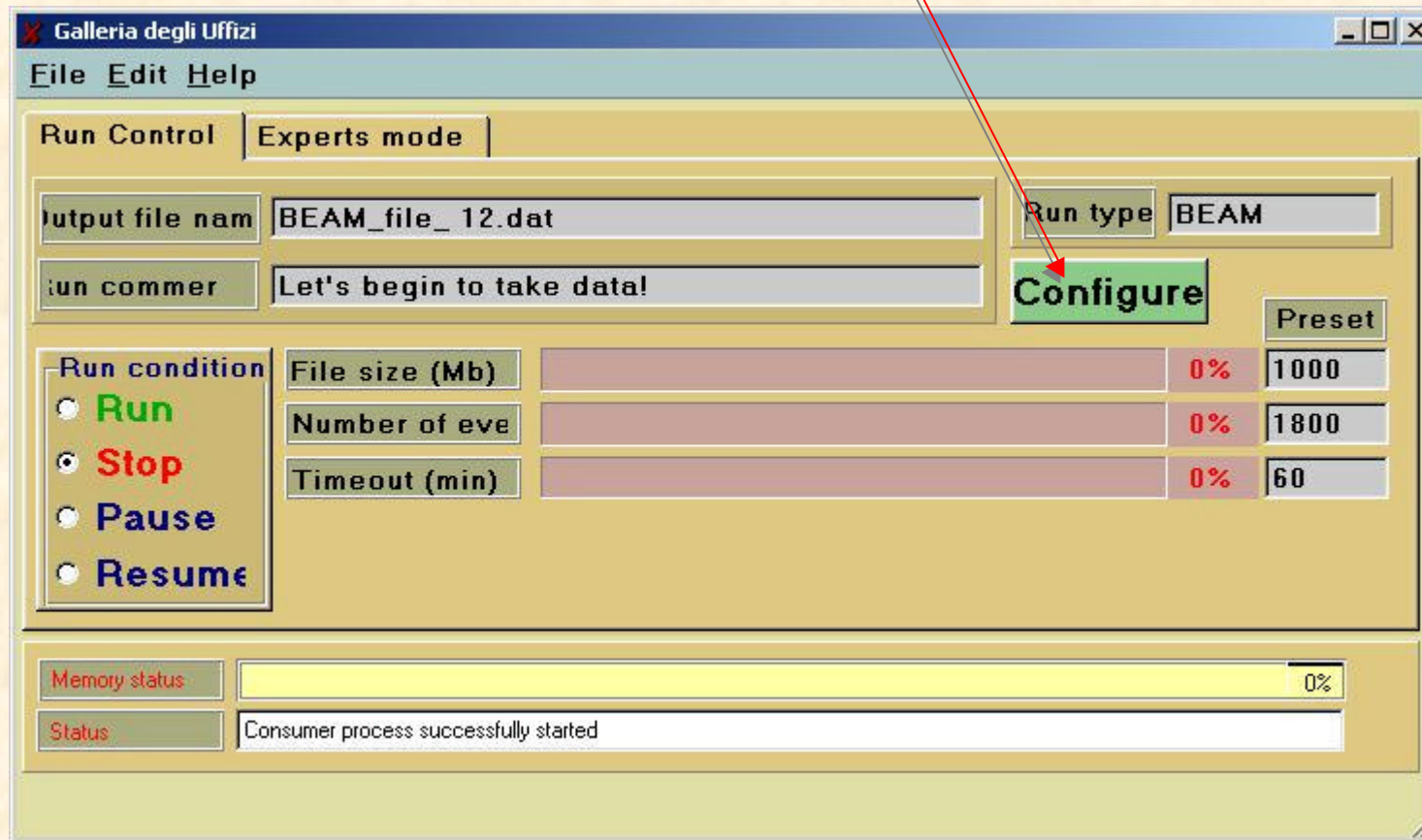


- **logger** : general logger
- **producer**: wait for interrupts, read PTA memories with data and fill shared memory
- **consumer**: continuously reads the shared memory, builds events and stores to disk





The system has an xml editor to change configuration of internal state



Galleria degli Uffici

File Edit Help

Run Control

Output file name

Run command

Run condition

- ☐ Run
- ☒ Stop
- ☐ Pause
- ☐ Resume

Memory status

Status

Uffizi

Save Quit

DAQ GPIB CAEN

Version 0.0.1 DaqMode OutputDataType BEAM

DaqHome	LogFile	Interspill	DataTaking	Max File Size	Max Events	Timeout
/home/uple/daq/	testlog1.txt	0	4	1000	1800	60

Branch 0 Branch 1 Branch 2

Bus 5 Slot 5 Status OFF

PTA

DataSource PTA MemoryLimit 0x1b9cc ClockDivision Prefetch OFF

Mezzanine

Master	SendUntriggeredData	SizeOfReceiveWindow	MaxDataWordsAllowed	MasterClockSource
0		0	0	0

Plane	PlaneID	BCDClockValue	BCDClockAdjustment	DataClockSelect	DataClockAdjustment
0	1	687			
1	2	831			

Detector 0

Status OFF Kill, Inject Masks

Type	# Rows	# Columns	ChipID
FPIX1	160	18	7

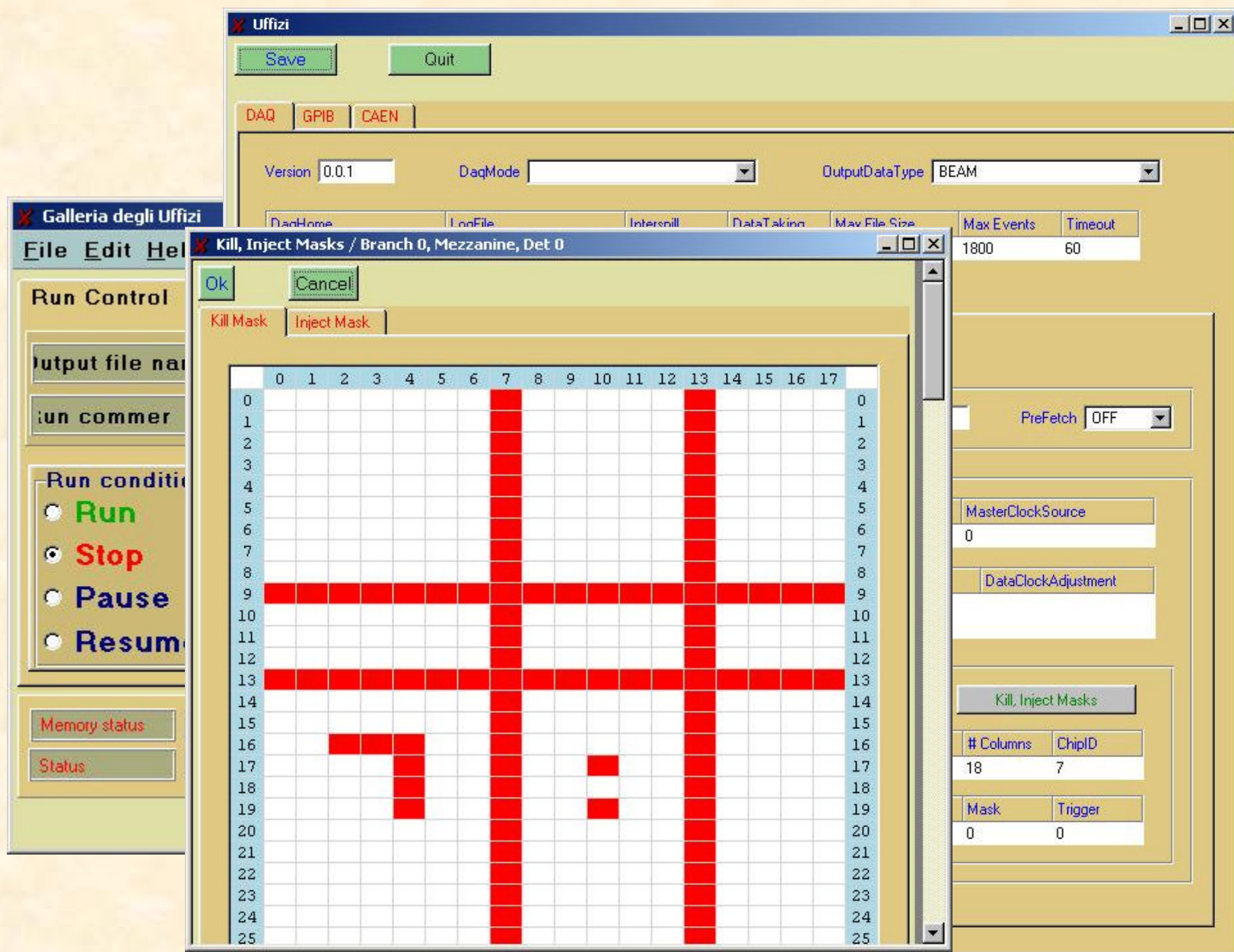
Mode	Lag	Mask	Trigger
0	63	0	0

Detector 1

Status ON Kill, Inject Masks

Type	# Rows	# Columns	ChipID
FPIX1	160	18	7

Mode	Lag	Mask	Trigger
0	63	0	0



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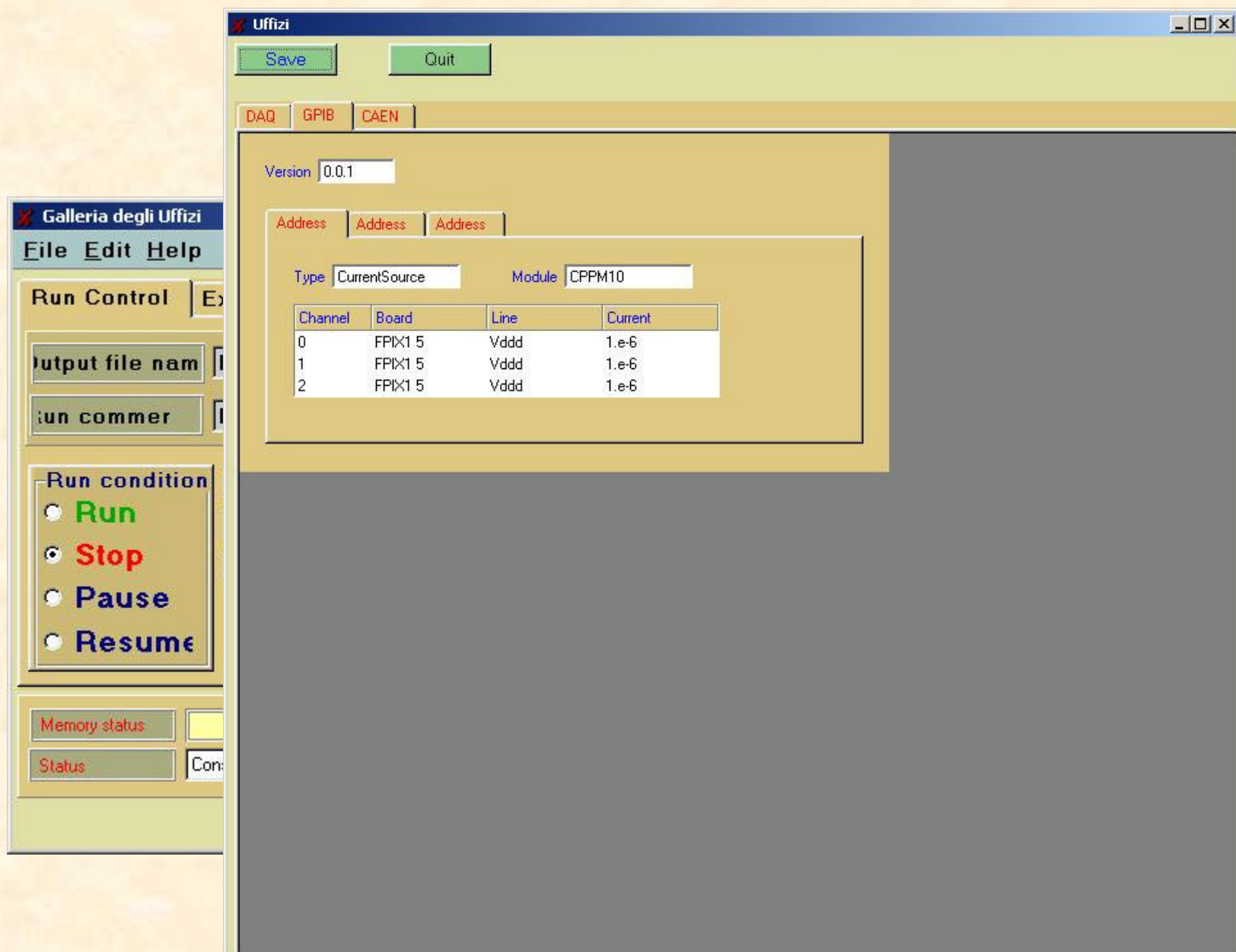
Mode	Lag	Mask	Trigger
0	63	0	0

Detector 1

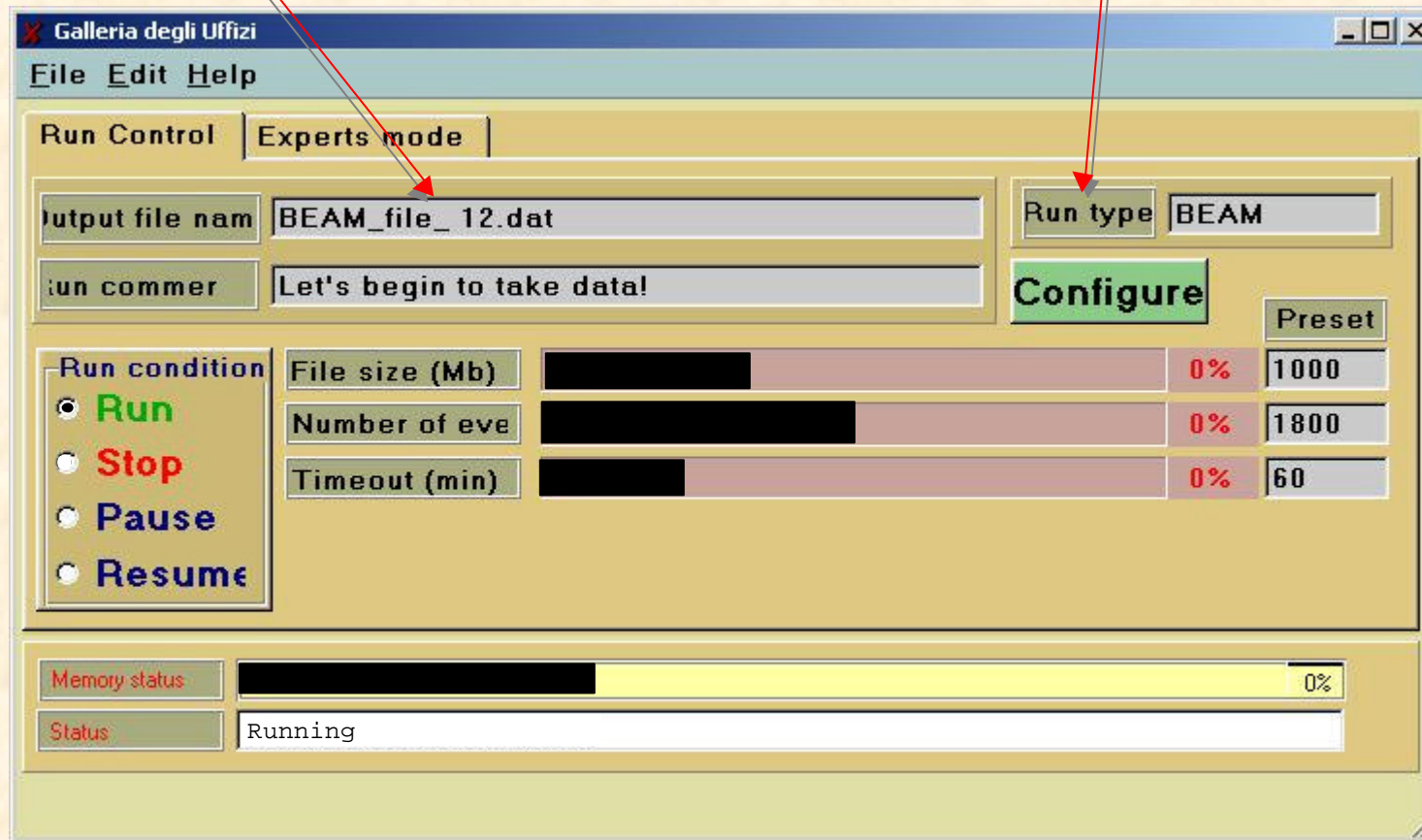
Status ON Kill, Inject Masks

Type	# Rows	# Columns	ChipID
FPIX1	160	18	7

Mode	Lag	Mask	Trigger
0	63	0	0



The output file name is dynamically composed by the “Run type” prefix and an automatically incremented run number



Current problems with hardware

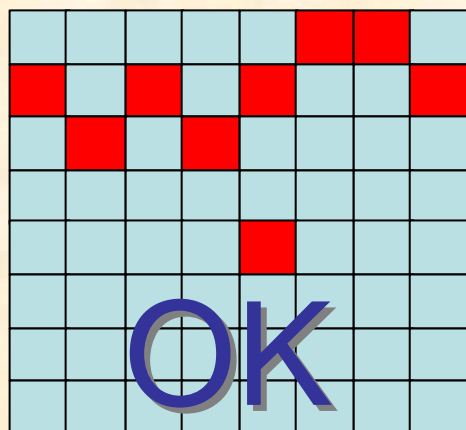
- **mezzanine**

the Long BCO counter sometimes goes in a locked state. This happens randomly under no clear set of circumstances.

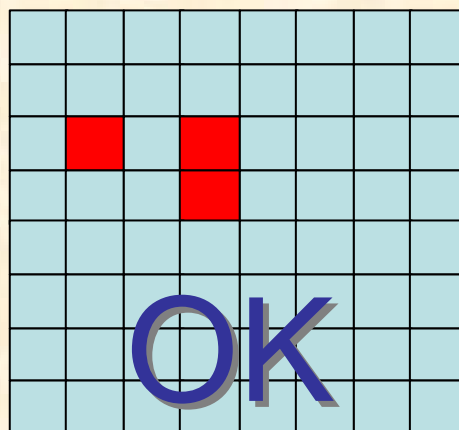
We have no idea how to restart it (even turning off power or resetting doesn't work)
Even if the counter works, independently of the number of enabled cells, above a certain rate (10 kHz) the counter gets locked again.

- **chip**

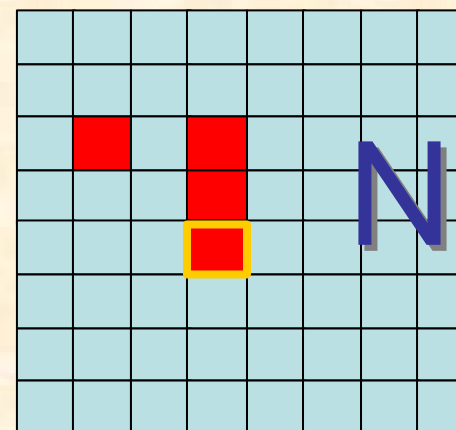
the stability of the chip depends upon the pattern of enabled cells. This seems to depend upon cells sharing the same column number.



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